

1. Overview

As described in previous chapters, the causes and mechanisms of semiconductor device failures are affected by various factors and are therefore very complicated. Toshiba enforces strict quality control in its semiconductor manufacturing processes based on comprehensive analysis of the factors affecting reliability as well as the problems that occur in the manufacturing process and after products have shipped. Although it is impossible to completely eliminate all failures, when a failure does occur, expeditious failure analysis is quickly used to identify the source of the problem and proper action is taken.

Some failures occur in the manufacturing process, others are detected in the inspection process, and many others occur with the passage of time in the field. Failure analysis is performed in all of these cases.

In addition to identifying the cause of failures and analyzing failure mechanisms, failure analysis also involves various chemical and physical techniques for extracting and controlling parameters affecting reliability, beginning with the earliest stages of the manufacturing process. The results are applied to the determination of process conditions and the development of process control technology. Thus failure analysis has become an important part of semiconductor manufacturing technology.

To correctly identify the causes and mechanisms of failures, various analytical instruments must be used according to prescribed analysis procedures. Therefore, failure analysis requires an analytical expertise based on a knowledge of chemistry and physics as well as an understanding of the physical characteristics of semiconductors.

When performing failure analysis, the following points must always be considered:

- (1) What are the symptoms of the failure, when and where did they appear, and is the failure repeatable? (Failure Mode)
- (2) Where is the failure located in the device and what kind of stress was applied at that location? (Failure Mechanism)
- (3) Has a similar failure ever happened in the field? Is the probability of the failure predictable from the mechanism model? (Statistical Analysis)
- (4) Efforts must be made to prevent recurrence of the failure by developing methods for controlling process parameters which affect reliability, providing feedback of information to the manufacturing process, and taking proper corrective action.
- (5) Failure analysis methods and strict reliability controls must be utilized to enable product reliability to be determined without the necessity for performing extensive evaluation tests.

2. Tools

Failure analysis of semiconductor devices requires high-precision analytical instruments capable of taking measurements of the order of microns and Angstroms. As well as being used to measure electrical characteristics for analysis purposes, such tools are often used to locate the source of failures and to determine failure mechanisms. Table 2.1 lists equipment used in failure analysis.

Table 2.1 Instrumentation used in failure analysis

	Instrument	Usage
Measure electrical characteristics	Curve tracer Oscilloscope Tester	Checking of breakdown voltage, leakage detection Checking of functions, checking of AC characteristics Checking of DC and AC characteristics, checking of functions
Find location of failure	Liquid crystal analyzer (polarization microscope) Emission microscope (EMS) Scanning laser microscope EB tester (strobe scanning electron microscope)	Hot spot detection Luminescent spot detection Operation analysis (OBIC/OBIRCH method) Operation analysis (voltage contrast)
Observe	Stereo microscope Metallurgical microscope Infrared microscope Scanning probe microscope (SPM) Scanning electron microscope (SEM) Transmission electron microscope (TEM) X-ray fluoroscope Ultrasonic flaw detector	Visual inspection Chip inspection Chip backside inspection Surface inspection Chip inspection Minute structure analysis Internal inspection Delamination and voids inspection
Analyze	Electron probe X-ray microanalyzer (EPMA) Auger electron spectroscope (AES) Secondary ion mass analyzer (SIMS) X-ray photoelectron spectroscope (XPS) Fluorescence X-ray analyzer Fluorescence microscope Fourier transformation infrared spectrometer (FTIR) Electron spin resonance detector (ESR) Electron beam diffractometer X-ray diffractometer Scanning infrared detector Thermal analyzer Gas mass analyzer	Elemental analysis, composition analysis Surface elemental analysis, status analysis Element identification, surface elemental analysis Surface elemental analysis, status analysis Impurity analysis, composition analysis Fluorescent material analysis Status analysis Electron status analysis Crystallization analysis Crystallization analysis, stress measurement Internal chip temperature distribution measurement Material analysis Material analysis
Prepare sample	Focused ion beam (FIB) Grinder/polisher Ion milling system	Sample preparation Sample preparation Sample preparation

3. Procedure

When performing failure analysis, it is best to take a systematic approach. An example is shown in Figure 3.1. Analysis should follow the flow shown in the example so that data sufficient for determining the failure mechanism can be collected.

Refer also to the failure analysis procedure shown in MIL-STD-883D, Method 5003.

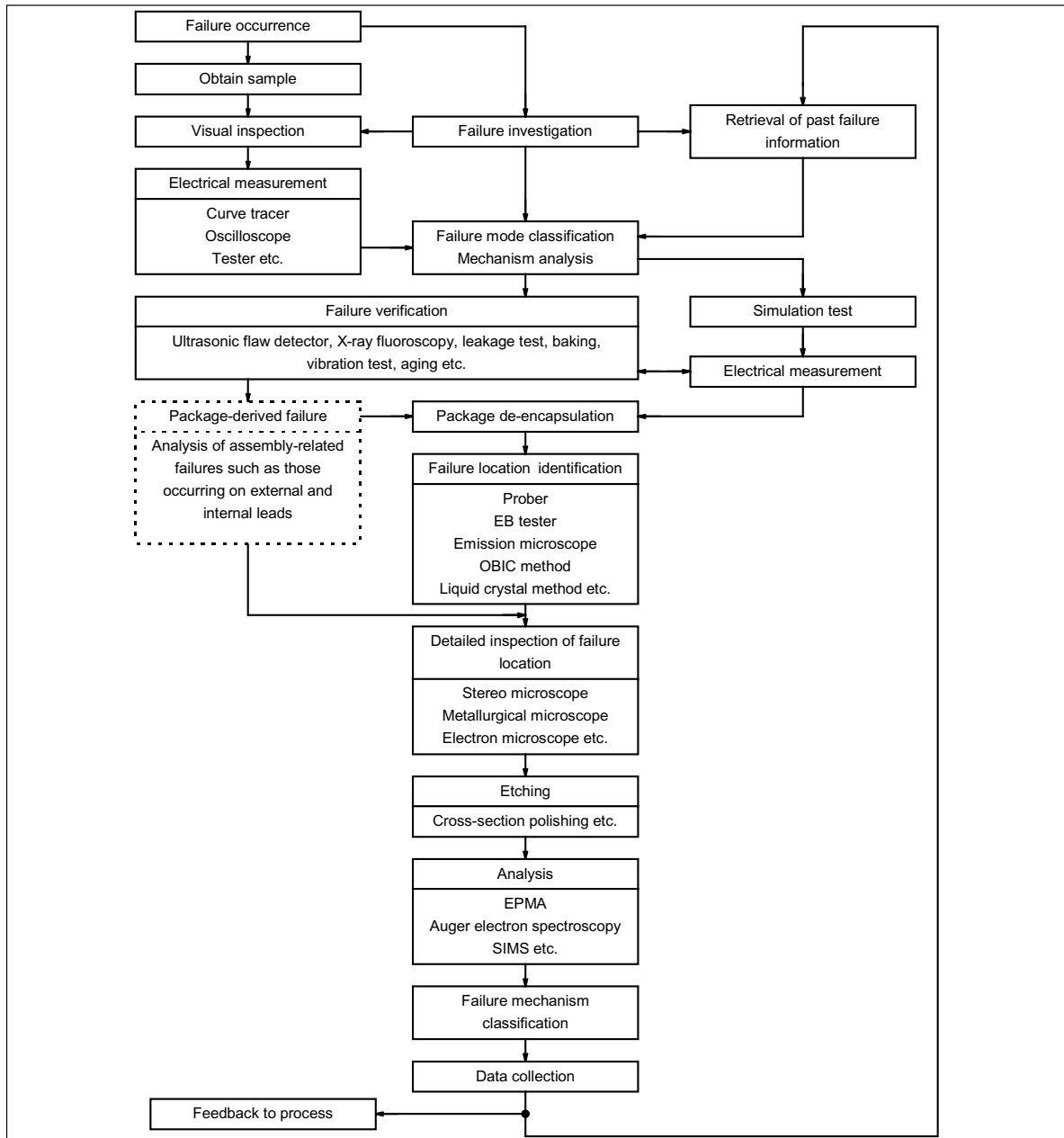


Figure 3.1 Failure analysis procedure

(1) Measuring electrical characteristics

In general, a curve tracer or similar equipment capable of measuring current-voltage characteristics is used to check for opens, shorts and breakdown voltage degradation. Also, an oscilloscope is handy for checking AC characteristics.

Testers, such as large universal testers for LSI, memory testers and linear IC testers, are used according to the type of device under test. Results are used to diagnose failures or to determine the location in the circuit of failures based on comparisons with specifications.

(2) Determining the failure location

The first step in failure analysis is to determine the failure location. There are several ways to do this. One is to find abnormal temperature distributions within the chip using a scanning infrared detector. Another is to find minute leakages using a liquid crystal analyzer to detect hot spots or an emission microscope to detect weak luminescence.

There are several methods for analyzing the operating state of a device. The EBIC method uses an electron microscope. The OBIC method or OBIRCH method use a scanning laser microscope to analyze the PN junction voltage. The voltage contrast method uses an EB tester to analyze the electrical potential of the wire.

(3) Observing with instruments

In addition to the metallurgical and stereo microscopes, the scanning electron microscope (SEM) and transmission electron microscope (TEM) are essential for identifying failure locations. An infrared microscope and X-ray inspection system can also provide important information. Recently, the scanning tunnel microscope (STM) and atomic force microscope (AFM), which are capable of providing atomic-level information, have been employed.

(4) Analyzing elements with instruments

Solid surface analysis is an important procedure in the investigation of semiconductor failures. The principle involves projecting an excitation source, such as an electron beam, ion beam or electromagnetic wave (e.g. an X-ray) onto the solid surface of the semiconductor material, as shown in Figure 3.2. The X-ray, secondary ion or Auger electron signals ejected by the excited material are then used for elemental and chemical state analysis of the material (or bulk). Table 3.1 summarizes the characteristics of the solid surface analysis method. Of the equipment listed in the table, the electron probe X-ray microanalyzer (EPMA), Auger electron spectroscope (AES) and secondary ion mass spectrometry (SIMS) analyzer are often used in the analysis of very small regions of the chip. The X-ray photoemission spectroscope and electron spectroscope are used for chemical analysis (XPS / ESCA) and the fluorescence X-ray spectroscope is used for elemental analysis of wide areas.

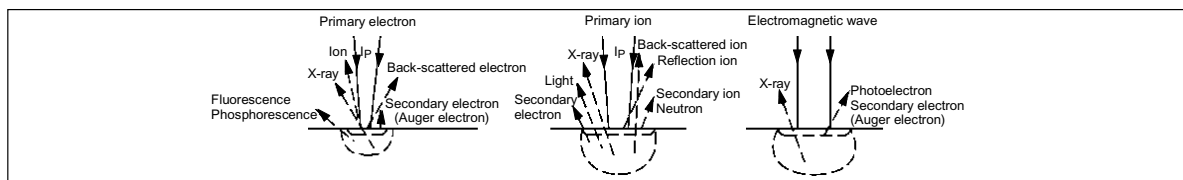


Figure 3.2 Interaction of ion, electron and photoelectron (X-ray) with solid surface¹⁾

(5) Other analysis

Surface and cross-sectional observations, and investigation of specific locations in the LSI (failure locations) are necessary in failure analysis. To prepare samples for these types of observation, a focused ion beam (FIB) system and precision polishing equipment are necessary.

Table 3.1 Comparison of surface analysis methods¹⁾

Excitation Source	Signal Source	Analysis Technique	Data Obtained	Features and Remarks	
Electron	Reflected primary electron	Low-speed electron energy spectroscopy (LEES)	Adsorption state	Uses low-energy electrons of several eV. Shows vibration state of adsorbed molecule.	
	Auger electron	Auger electron spectroscopy (AES)	Elemental analysis, bonding energy, state analysis based on chemical effects	Uses electron beam of up to about 3 eV. Surface analysis with small beam of less than 1 μm is also possible.	
	Ion	Electron impact drift method		Elemental analysis of adsorbed matter	Impact of minute current applied to surface removes adsorbed ions, performing mass separation.
		Spark-type solid mass analysis		Microelemental analysis	
	Characteristic X-ray	Analysis using electron probe X-ray microanalyzer (EPMA)		Elemental analysis of minute areas	Commonly used in microanalysis. Detectable depth is about 1 μm.
	Light (ultraviolet) (visible)	Luminescence spectroscopy		Elemental analysis	
Ion	Secondary electron	Ion-neutralization spectroscopy (INS)	Surface electron state, adsorption state	Elemental analysis by Auger electron spectroscopy (under study)	
	Reflected ion	Ion-scattering spectroscopy (ISS)	Elemental analysis of weight of single atom	Using low-speed ion (1–several eV) separates energy of reflected primary ion.	
	Back-scattered ion	Back-scattering (IBS)	Composition, elemental analysis, distribution	Using He ⁺ of several MeV measures energy of back-scattered He ⁺ ion.	
	Secondary ion	Secondary ion mass analysis (SIMS)	Microanalysis, depth distribution	Thin film, surface analysis, microanalysis of bulk, concentration depth distribution	
	Characteristic X-ray	Ion excitation X-ray analysis	Elemental analysis	Currently under study	
X-ray, Ultraviolet ray	Photoelectron	Photoelectron spectroscopy (XPS) Vacuum ultraviolet electron spectroscopy (UPS)	Elemental analysis, electron coupling energy	By measuring photoelectron energy detects electron coupling energy and analyzes elements.	
X-ray, Soft X-ray	Secondary X-ray	Fluorescence X-ray analysis	Elemental analysis		
		Soft X-ray analysis	Electron state	By irradiating with a soft X-ray (10–10 ³ eV) measures electron state of atom.	

LEES: low-energy electron spectroscopy
ISS: ion-scattering spectroscopy

INS: ion-neutralization spectroscopy
IBS: ion back-scattering

As soon as a failure sample is obtained, its history is investigated. Any related information, including manufacturing lot information (manufacturing date and length of storage), details concerning the failure (correlation to lot, whether the failure is total or intermittent, failure rate), operating conditions (circuit, thermal stress, mechanical stress) and environmental conditions (temperature, humidity, location, atmosphere) should be collected and used to determine the failure mechanism. This information can then also be used for simulation tests. You should also have known good samples on

hand against which the failed device can be compared.

During the visual inspection the exterior of the package of the failed device is examined visually or with a stereo or metallurgical microscope. A number of failure causes can be detected in this way, such as cracks in the package, metal migration between leads, mechanical damage or rust on the leads. Elemental analysis, which is one part of solid surface analysis as described above, is applied as needed when estimating the cause of failure.

Next, electrical characteristics are measured using a curve tracer, oscilloscope and other testers, and recorded. The quickest way to obtain failure mode data is by using a curve tracer.

The failure mode and failure mechanism of the device are identified, based on a summary of the investigation results, a visual inspection and electrical characteristic measurements, as well as on any past history or statistical data. There are three major failure mode classifications: opens, shorts and degradation. Subsequent testing and analysis are based on these failure mode and failure mechanism judgments.

For hermetically-sealed devices, a hermeticity test is performed, followed by an analysis of the sealing gas if necessary.

Before the device is de-encapsulated, baking, retesting, vibration testing etc. are performed as needed to determine the failure mechanism. Also an internal examination by X-ray fluoroscopy should be carried out to check bonding wires and leads for opens or shorts (this also should be carried out before de-encapsulation).

A de-encapsulation method is selected based on the presumed failure mechanism, with the aim of enabling the semiconductor chip to be observed and analyzed. If the device is improperly de-encapsulated, the necessary data cannot be obtained and the cause of failure cannot be determined. Therefore, special precautions must be taken during de-encapsulation.

De-encapsulation methods include: wet (dissolving using chemicals), dry (mechanical removal) and incineration (using a plasma reactor).

The wet de-encapsulation method is frequently used with plastic packages. The method of incineration by plasma reactor allows the chip to be exposed smoothly without the use of hazardous chemicals; however, the required equipment is expensive.

For ceramic and metal packages, dry (mechanical) de-encapsulation is preferred, as no special equipment or tools are required.

The de-encapsulated sample should be analyzed immediately. However, if this is not possible, the device should be stored in a low-humidity environment such as a desiccator to prevent contamination or damage.

The most convenient and simple way of observing internal features in detail is with a metallurgical microscope. A stereo microscope can be used to examine the condition of the wire bonds and die bonds. A scanning electron microscope can be used to make observations and take photographs at high magnification.

If the cause of failure cannot be determined by microscopic observation alone, elemental analysis and state analysis at the defective location must be performed. Optimized methods and equipment such as EPMA, AES and SIMS are used accordingly.

If the location of the failure cannot be determined by internal state observation, other techniques such as voltage contrast measurement using an EB tester, emission microscope analysis, the liquid crystal method or the OBIC method can be used.

In addition, layer removal or cross-sectioning of the failed sample using wet etching, polishing or FIB analysis are used to detect and examine the failure location and thereby determine the failure mechanism.

Results obtained from the above analysis methods are fed back to the manufacturing process, and are also stored in a database for the purpose of improving device reliability.

4. Examples

In this section the major failure analysis methods are described using the following 16 examples:

- (1) Failure identification using an emission microscope
- (2) Die backside analysis using an infrared emission microscope (IR EMS)²⁾
- (3) Failure identification using an emission microscope and an EB tester
- (4) Via hole open identification using a scanning electron microscope (SEM)
- (5) Gate oxide breakdown analysis using an SEM³⁾
- (6) Interlayer particle analysis
- (7) Al metallization grain size and residual stress analysis
- (8) High-resolution analysis using a TEM
- (9) TEM cross-sectional analysis of failures identified using OBIC (optical beam-induced current)⁴⁾
- (10) Analysis of fine particles in LSI using Auger electron spectroscopy -1
- (11) Analysis of fine particles in LSI using Auger electron spectroscopy -2
- (12) Chemical status analysis using XPS
- (13) Wafer surface contamination analysis using a TOF-SIMS (time-of-flight secondary ion mass spectrometer)⁵⁾
- (14) Junction analysis using an SCM (scanning capacitance microscope)⁶⁾
- (15) Bonding pad corrosion analysis
- (16) Analysis of surface-mount device package crack due to reflow

(1) Failure identification using an emission microscope

Failure mode: Standby leakage failure during reliability test

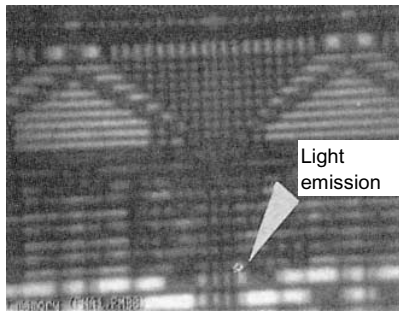
Analysis: Observation was carried out using an emission microscope. Light emission was detected from the N-channel MOS in the address decoder circuit (see Figure 4.1 (a)).

A crystal defect was found after removing layers on the Si-substrate at the point at which light was emitted (see Figure 4.1 (b)).

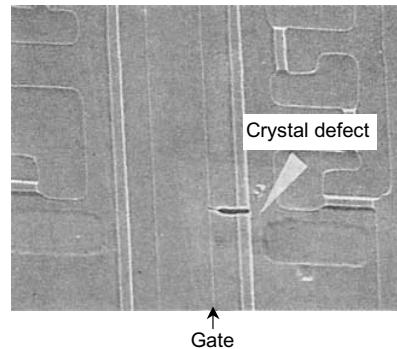
With another sample, light emission was detected from the N-channel MOS in the AD converter front stage (see Figure 4.2 (a)).

Gate oxide film breakdown was found after the removal of layers on the Si-substrate (see Figure 4.2 (b)).

Mechanism: N-channel MOS leakage due to crystal defect and gate oxide film breakdown (TDDB)

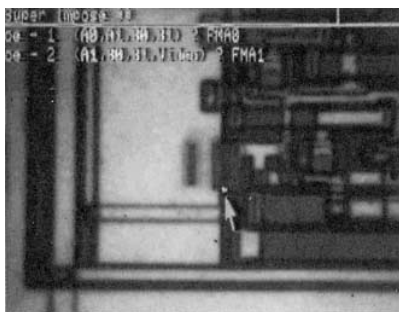


(a) Light emission from address decoder circuit

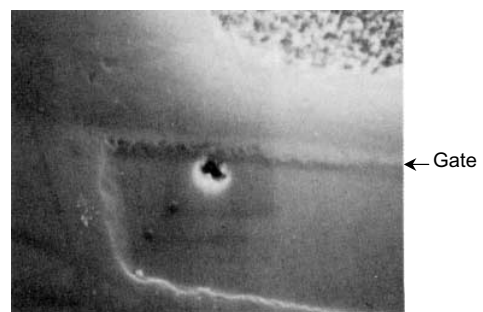


(b) Crystal defect at point where light is emitted

Figure 4.1 Standby leakage failure due to crystal defect



(a) Light emission from AD converter front stage circuit



(b) Oxide film breakdown at point where light is emitted

Figure 4.2 Standby leakage failure due to gate oxide film breakdown

(2) Die backside analysis using an infrared emission microscope (IR EMS) ²⁾

Failure mode: Characteristic failure during board mounting process

Analysis: Light emission was detected from the backside of the Si die when it was observed after mirror polishing using an IR EMS (see Figure 4.3). Oxide film breakdown in the MOS capacitor was found when it was observed after de-encapsulation using a scanning microscope (SEM) (see Figure 4.4).

Mechanism: Oxide film breakdown due to ESD

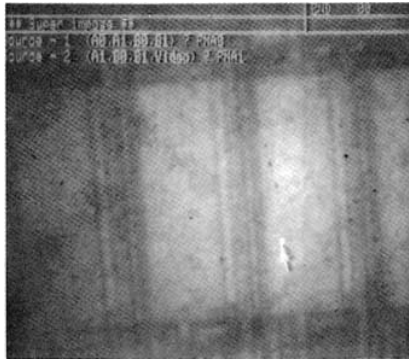


Figure 4.3 Overlapping of emitted image and pattern image (emission spot indicated by arrow)

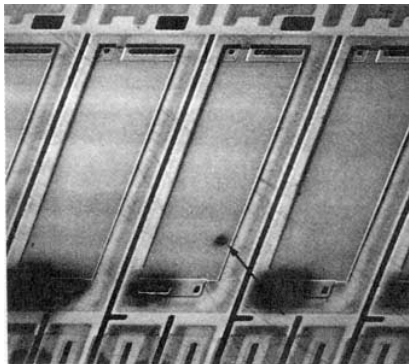


Figure 4.4 Oxide film surface after de-encapsulation and removal of layers on oxide film (scanning electron microscope image)

(3) Failure identification using an emission microscope and an EB tester

Failure mode: Function leakage failure during reliability testing

Analysis: The IC was set to standby mode and its light emission was observed from multiple angles using an emission microscope. An EB tester was then used to identify wire opens. A sample was prepared using an FIB and Al opens due to foreign matter were found.

Mechanism: Al metallization near-disconnect due to particulate was completely disconnected by stress.

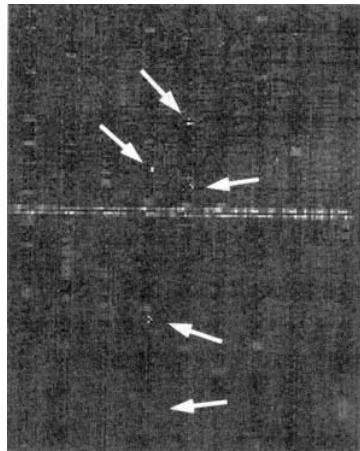


Figure 4.5 EMS strobe image

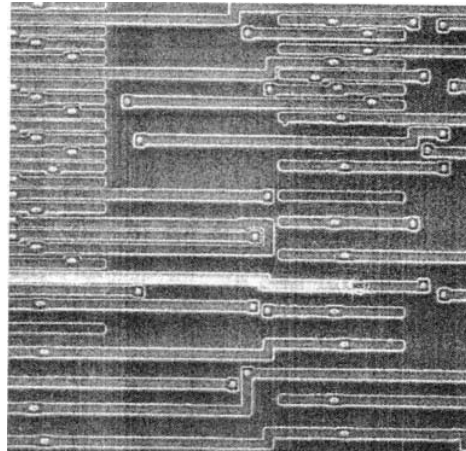


Figure 4.6 EB tester Image

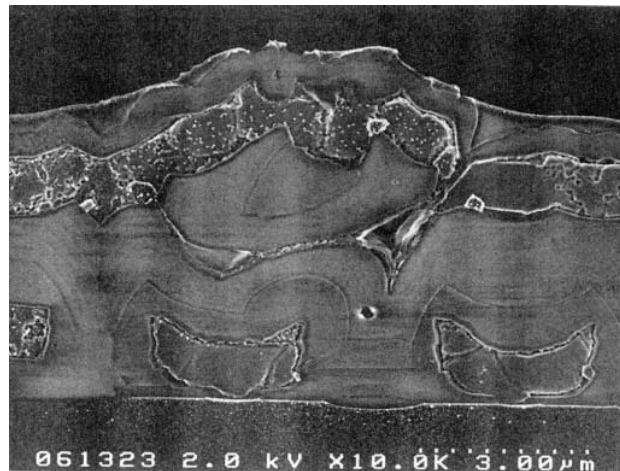


Figure 4.7 Cross-sectional image of open sites

(4) Via hole open identification using a scanning electron microscope (SEM)

Failure mode: Via contact open failure

Analysis: Defective via contact opens were identified using the SEM charge-up technique; a cross-section was prepared using an FIB and observed.

Mechanism: Via contact open due to insufficient via RIE etching

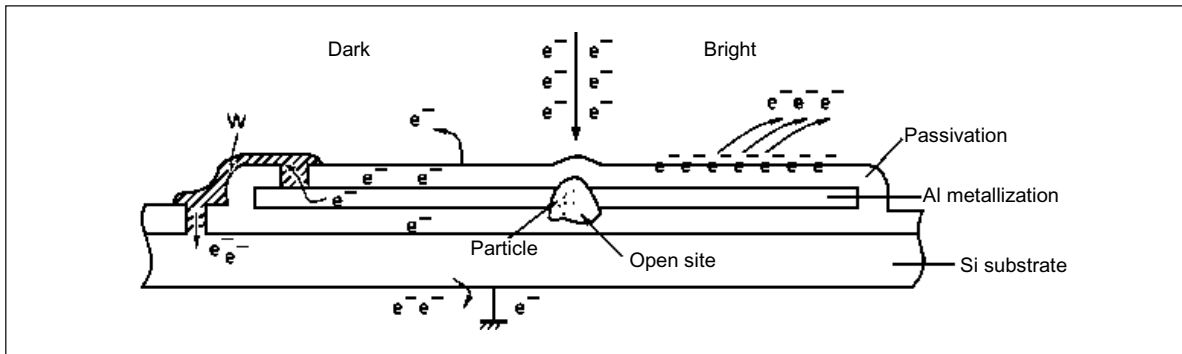


Figure 4.8 Open site identification method

When observed with an SEM, the charge-up condition of the Al metallization where it is insulated from the substrate differs from that where it is grounded. Therefore, an open site is detected because the contrast on either side of the site of the open is different.

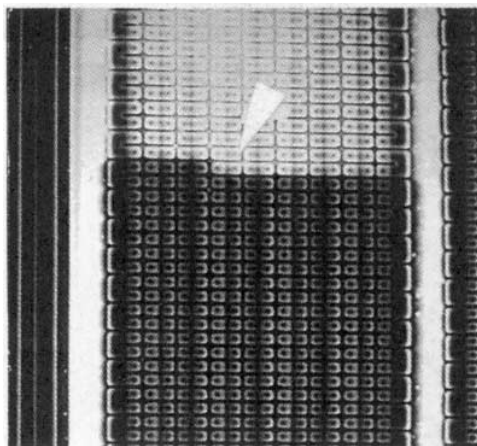


Figure 4.9 Identification of open site

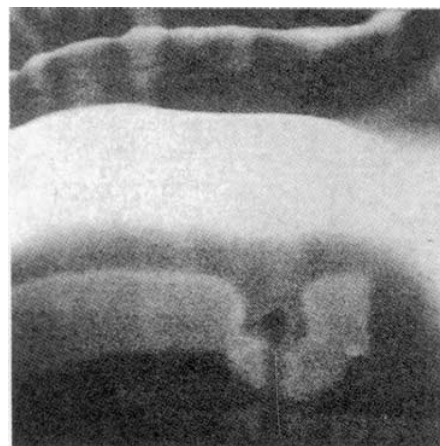


Figure 4.10 Via contact cross-section

(5) Gate oxide breakdown analysis using an SEM³⁾

Failure mode: Standby leakage failure during high-temperature lifetime test

Analysis: Leakage between gate polysilicon and substrate was observed using the SEM charge-up technique (see Figure 4.11) after removing the wires connected to the gate polysilicon (see Figure 4.12).

Also, gate oxide film breakdown was observed after removal of gate polysilicon (see Figure 4.13).

Mechanism: Time-dependent dielectric breakdown (TDDB)

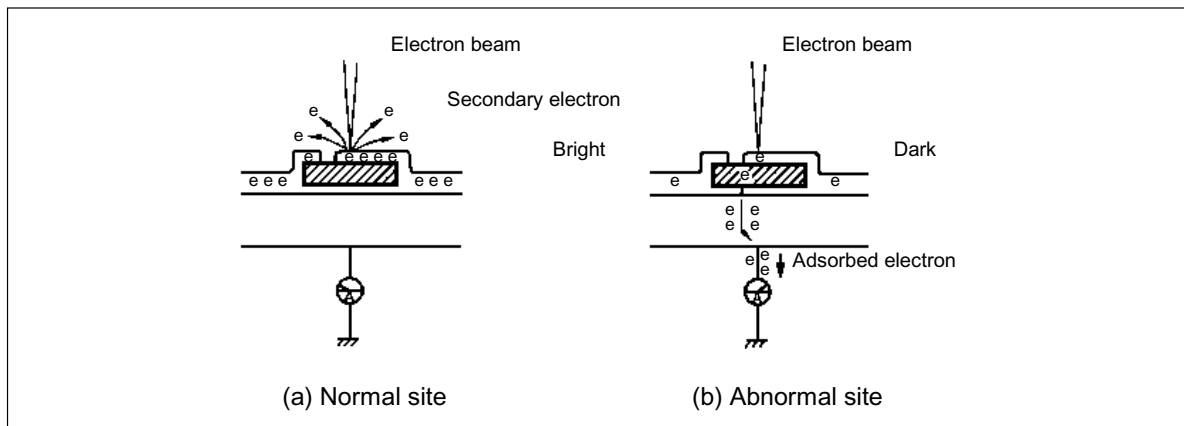


Figure 4.11 Identification of gate oxide film breakdown site using an SEM³⁾

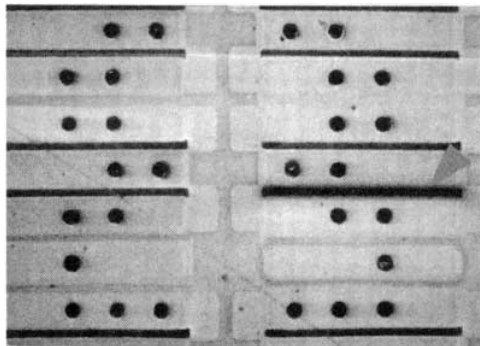


Figure 4.12 Identification of faulty gate polysilicon as indicated by leakage between polysilicon and substrate

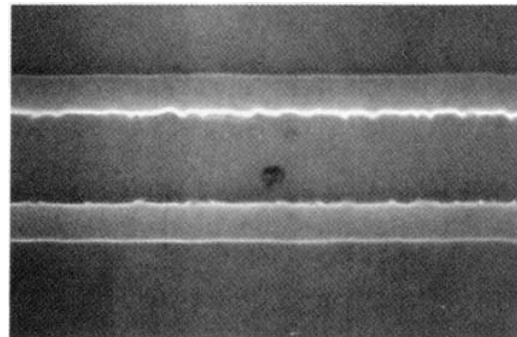


Figure 4.13 Gate oxide film breakdown site

(6) Interlayer particle analysis

Failure mode: Al metallization open due to particles

Analysis: Disconnected Al metallization opens were identified using the SEM charge-up technique, and a cross-section was prepared using an FIB and observed. The particle was identified using EPMA.

Mechanism: Al metallization was disconnected because a particle was introduced from the machine used in the interlayer processing step.

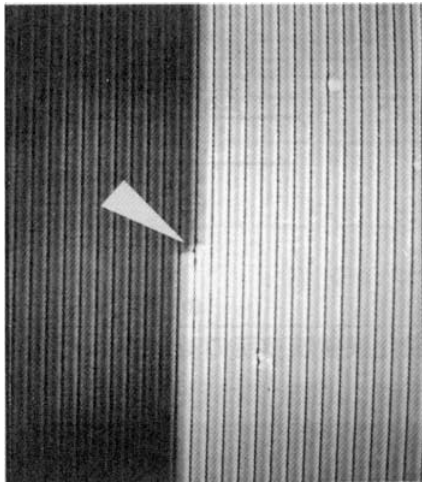


Figure 4.14 Identification of open site



Figure 4.15 SEM image of particle

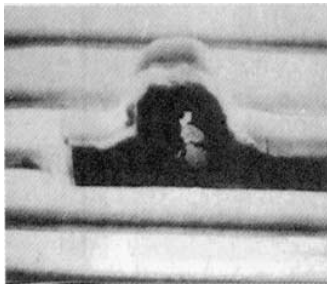


Figure 4.16 SEM image

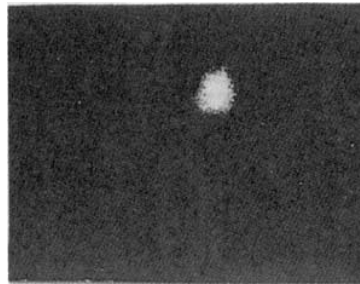


Figure 4.18 EPMA Fe X-ray image

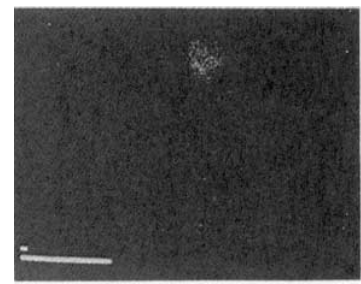


Figure 4.17 EPMA Cr X-ray image

(7) Al metallization grain size and residual stress analysis

Purpose: The grain size and residual stress of Al metallization have an effect on electromigration and the stress migration lifetime.

Analysis examples of Al grain size and residual stress due to wafer temperature during Al deposition and anneal processing after deposition are shown.

Analysis: The Al grain was observed with a TEM and the grain size was measured. Al residual stress was measured using X-ray diffraction.

Result: The residual stress increased when the wafer temperature rose during Al deposition.

However, once Al deposition had ceased, continuing increase in the wafer temperature caused the grain size to increase, so that the residual stress remained at a constant level.

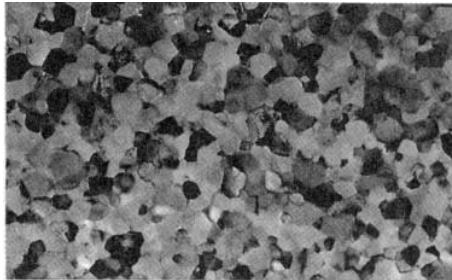


Figure 4.20 TEM image before Al anneal processing

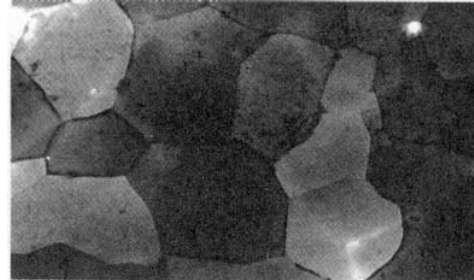


Figure 4.19 TEM image after Al anneal processing

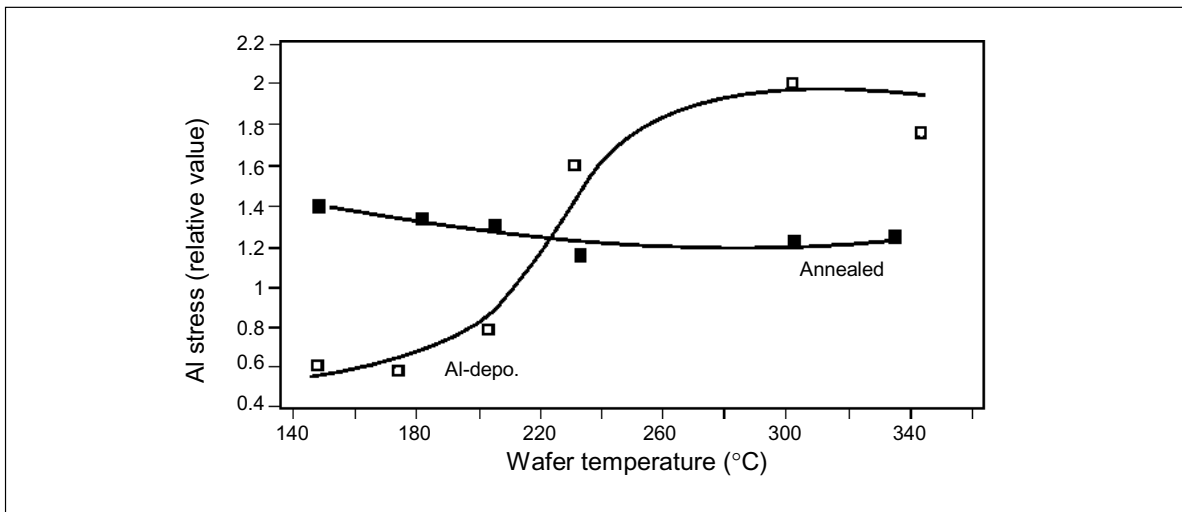


Figure 4.21 Relationship between Al film residual stress and Al deposition temperature

(8) High-resolution analysis using a TEM

Purpose: The surface condition of the Si substrate, the thickness of the SiO₂ and SiN thin films and their shape all affect dielectric breakdown strength and reliability. Advances in device integration and thin film technology have made it necessary to evaluate and analyze these factors at the atomic level.

Analysis: Thin film and its interface were observed at ultra-high resolution using a TEM.

Result: Natural oxide film was formed on the Si substrate surface due to chemical treatment.
 When the surface was treated with chemical A, natural oxide film with a thickness of 0.1 nanometer or less was formed.
 The cross-sectional structure of ONO film was analyzed. It was found that ONO film several nanometer thick could be formed with good reproducibility.

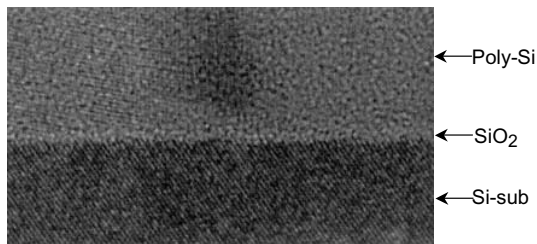


Figure 4.22 Natural oxide film formed by chemical A on substrate surface

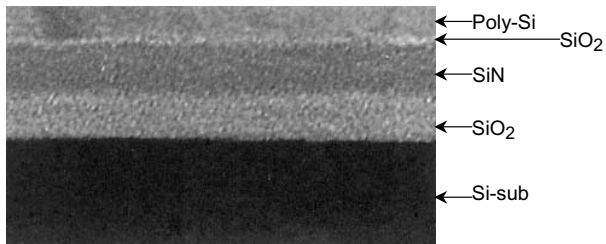


Figure 4.23 Cross-sectional structure of ONO film

(9) TEM cross-sectional analysis of failures identified using OBIC (optical beam-induced current) ⁴⁾

Purpose: OBIC is useful for identifying failures (e.g. leakage) for products in the early stages of development, since it allows bias-free measurement. In addition, observation with a TEM is necessary for a full understanding of the structure of small devices and thin-film devices. OBIC and TEM were used for the identification and observation of failures so that their nature could be clarified.

Analysis: Gate leak failure was identified using OBIC. A sample was then prepared using an FIB and observed using a TEM. High-precision FIB (focused ion beam) positioning was achieved by repeated FIB deposition marking and OBIC measurement.

Result: The gate oxide film at the failure site identified using OBIC had been damaged. Leakage was observed in the form of Poly-Si entering through the damaged gate oxide film.

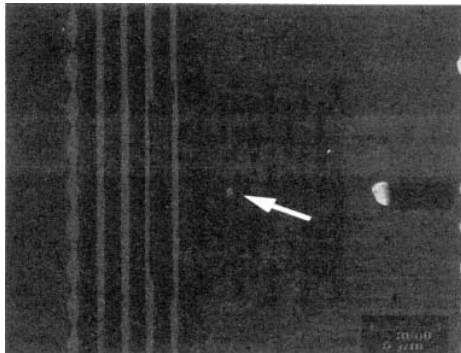


Figure 4.24 OBIC image (high-precision FIB positioning was achieved by FIB deposition marking)

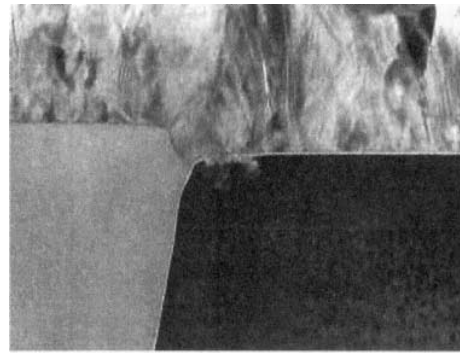


Figure 4.25 TEM cross-sectional image of light-emitting section



Figure 4.26 TEM image (enlarged): Poly-Si has entered through damaged gate oxide film.

(10) Analysis of fine particles in LSI using Auger electron spectroscopy -1

Purpose and analysis: Threadlike foreign matter in the LSI was observed (see Figure 4.27).

Result: A cross-sectional image of the foreign matter observed using an SEM is shown in Figure 4.28.

As a result of Auger electron surface analysis, Ti and Al were detected in the foreign matter.

The foreign matter was found to be metallization residue on which passivation film was deposited (see Figure 4.29).

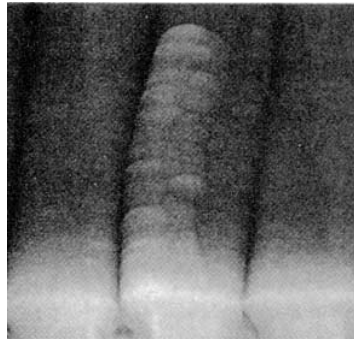


Figure 4.27 SEM image

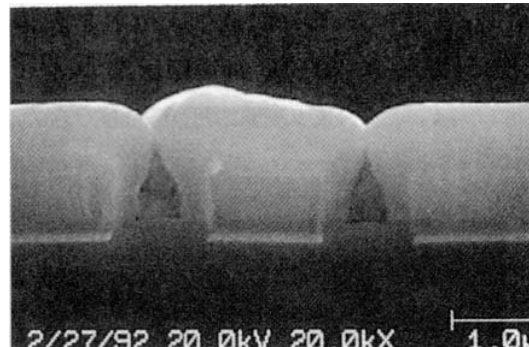
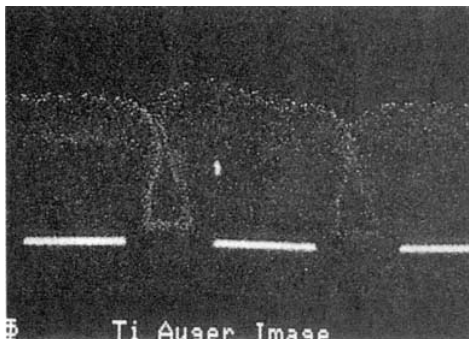
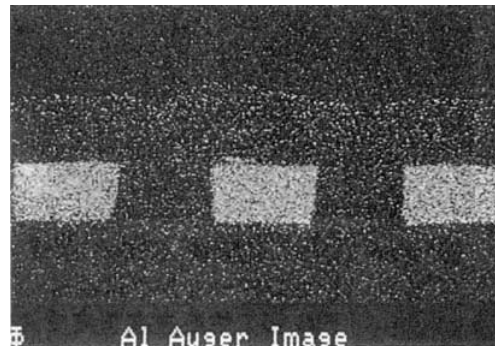


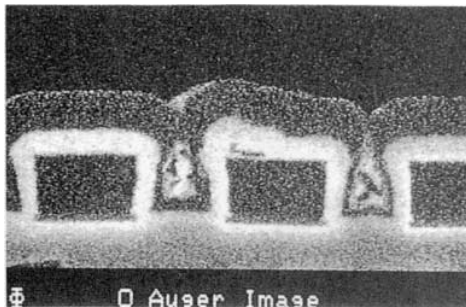
Figure 4.28 Cross-sectional SEM image



a) Auger electron image of Ti



b) Auger electron image of Al



c) Auger electron image of O

Figure 4.29

(11) Analysis of fine particles in LSI using Auger electron spectroscopy -2

Purpose and analysis: After surface abrasion, film-like foreign matter was observed around the contact hole (see Figure 4.30).

Result: As a result of Auger electron qualitative analysis, Si was detected in the foreign matter. The foreign matter was found to be Poly-Si from the bit line contact hole deposited between BPSG layers during the CMP process of the BPSG.

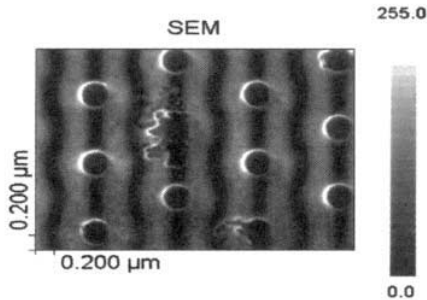


Figure 4.30 SEM image

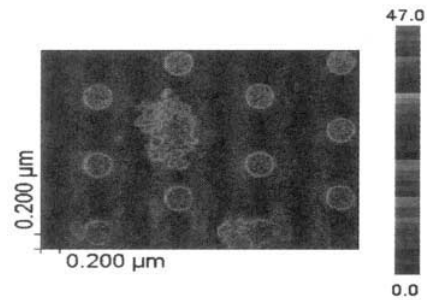


Figure 4.31 Image of O+Si

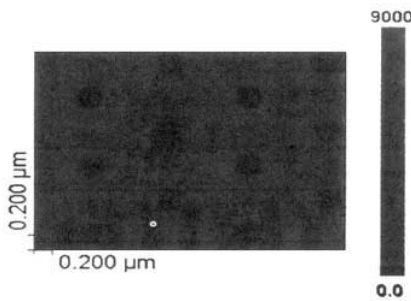


Figure 4.32 Image of O

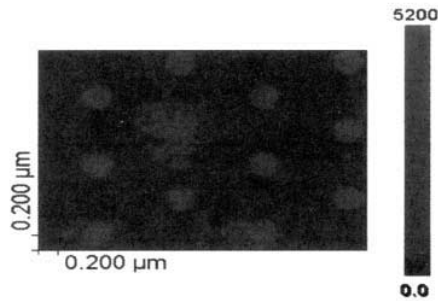


Figure 4.33 Image of Si

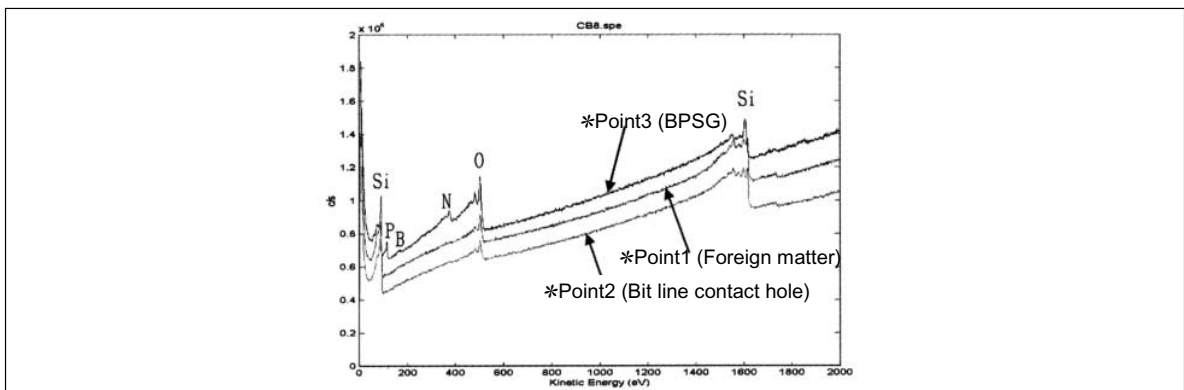


Figure 4.34 Auger spectrum

(12) Chemical status analysis using XPS

Purpose and analysis: After the polyimide had been etched using $\text{CHF}_3/\text{CF}_4/\text{O}_2/\text{Ar}$ gas, it was determined whether or not it would be possible to remove the damaged layer (CF_x) formed on the polyimide surface with O_2 asher.

Result: As shown in Figure 4.36 it was found that F forms a C-F type bond when the underlayer is Si, and an Al-F type bond when the underlayer is Al.

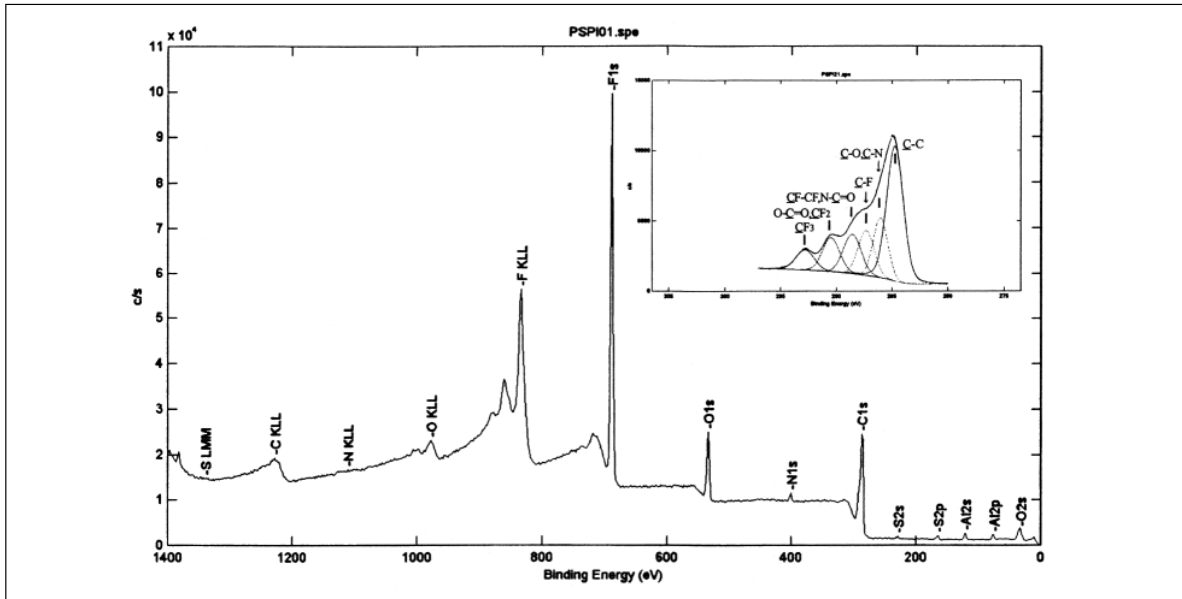


Figure 4.35 Result of polyimide surface qualitative analysis after RIE (reactive ion etching)

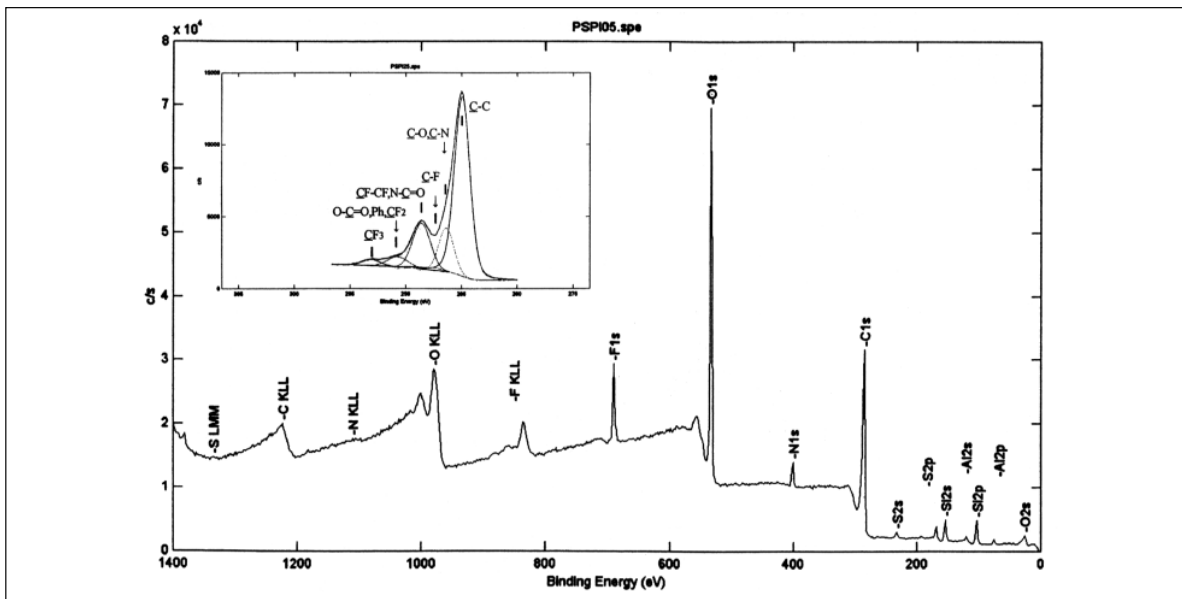


Figure 4.36 Result of polyimide surface qualitative analysis after RIE+ O_2 asher

(13) Wafer surface contamination analysis using a TOF-SIMS (time-of-flight secondary ion mass spectrometer)⁵⁾

Purpose: Surface contamination must be evaluated accurately because wafer surface contamination can cause degradation of the oxide film breakdown voltage and crystal defects.

Analysis: Contamination of the first atomic layer of the Si wafer surface was analyzed using a TOF-SIMS.

Principle of analysis: An element is identified by irradiating the sample with a pulsed ion beam and measuring the time it takes for the secondary ion from the sample to reach the detector. It is possible to perform highly accurate analysis of mono-atomic layer surface contamination within a specific area.

Result: Contamination with approximately 10^{11} atoms/cm² of Al and Fe was detected on the mono-atomic layer surface. Various organic compounds were also detected.

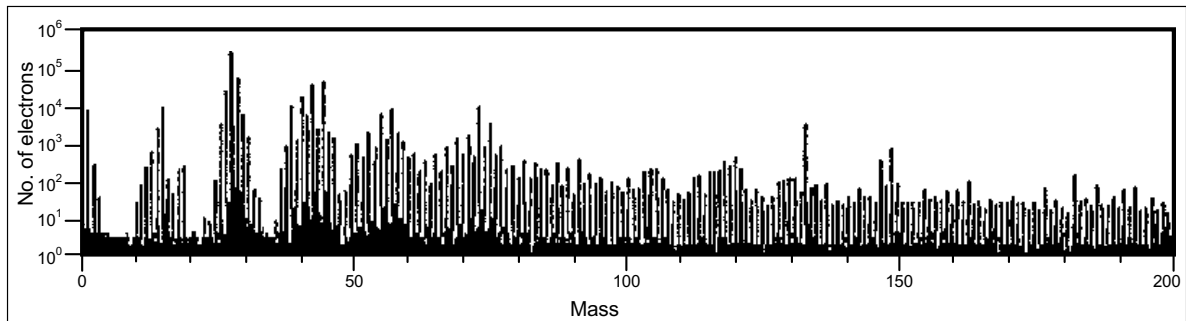


Figure 4.37 Si wafer mono-atomic layer surface mass spectrum taken using a TOF-SIMS

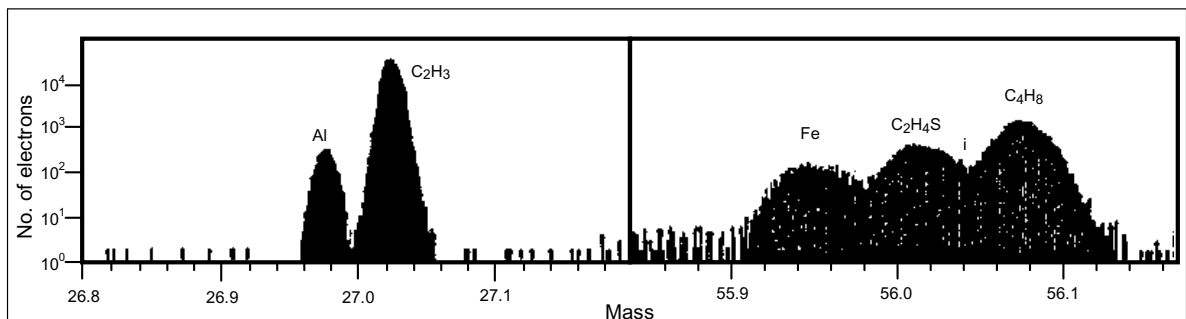


Figure 4.38 Enlargements of spectrum shown in Figure 4.37

(14) Junction analysis using an SCM (scanning capacitance microscope)⁶⁾

- Purpose:** The variation in diffusion depth in junctions which have been created by diffusion in the substrate can be observed by observing capacitance variation using an SCM. This is particularly effective for measuring local X_j or offset.
- Analysis:** The cross-sectional structure of a 16-MB DRAM trench was observed using an SCM.
- Result:** An N-layer had formed along the trench. Also, an offset was observed at the transfer gate.

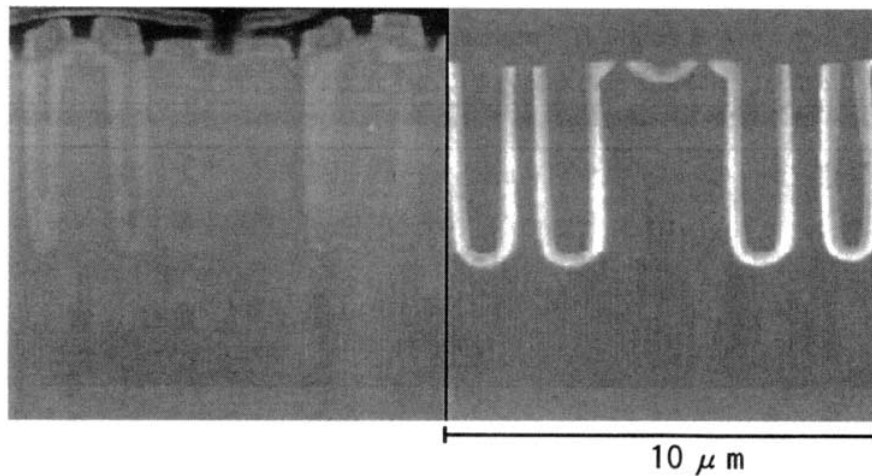


Figure 4.39 Trench (left: AFM image / right: SCM image)

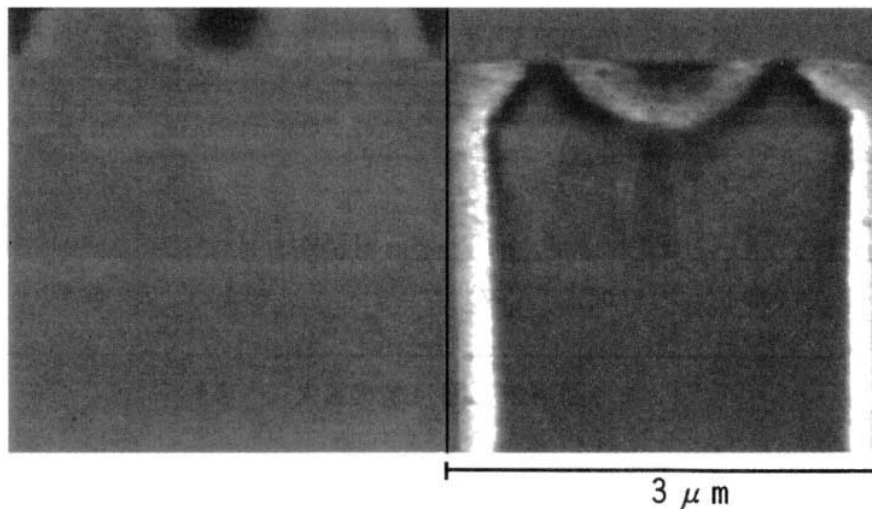


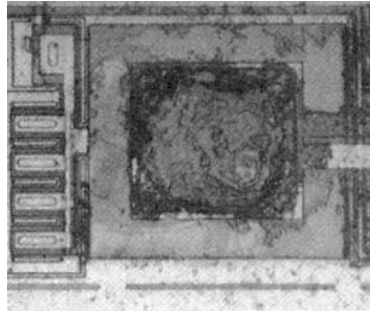
Figure 4.40 Transfer gate (left: AFM image / right: SCM image)

(15) Bonding pad corrosion analysis

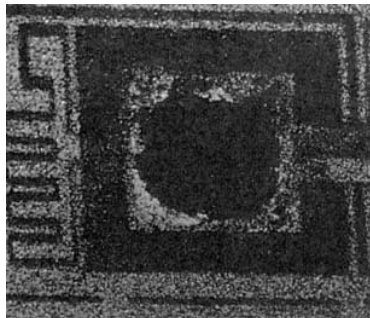
Failure mode: Open failure after humidity resistance test

Analysis: Abnormality was detected in an electrically open bonding pad after the molding resin was removed (see Figure 4.41 a)). As a result of EPMA analysis, Al melting was confirmed and Cl impurity was detected (see Figure 4.41 b) and c)).

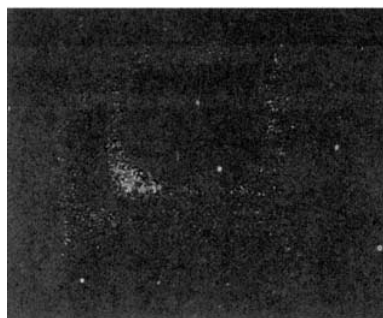
Mechanism: Bonding pad Al corrosion due to Cl contamination.



a) Microscope image of pad with open failure



b) Al X-ray image of a)



c) Cl X-ray image of a)

Figure 4.41 Example of bonding pad Al corrosion analysis

(16) Analysis of surface-mount device package crack due to reflow

Failure mode: Package cracks and bonding open due to VPS reflow after moisture absorption

Analysis: Formation of package cracks starting from the chip edge was confirmed by ultrasonic flaw detection, X-ray fluoroscopy and cross-sectional observation.

Mechanism: Internal moisture evaporated due to thermal stress during VPS. The vapor pressure exceeded the breakdown strength of the mold resin, causing the package to crack. The package cracks in turn caused the wire open (disconnection).

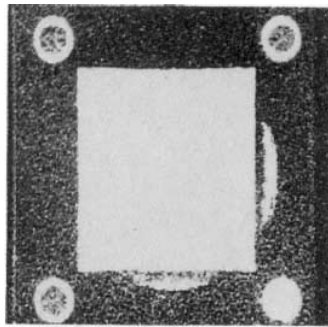


Figure 4.42 Observation using ultrasonic flaw detector

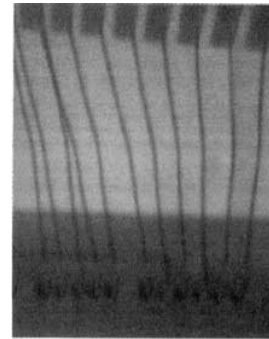


Figure 4.43 Observation using X-ray fluoroscopy (check for wire opens)

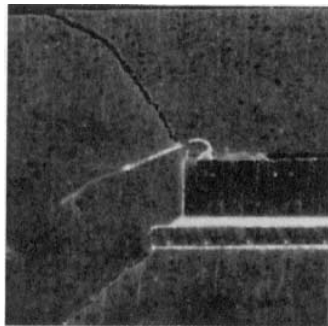


Figure 4.44 Cross-sectional observation

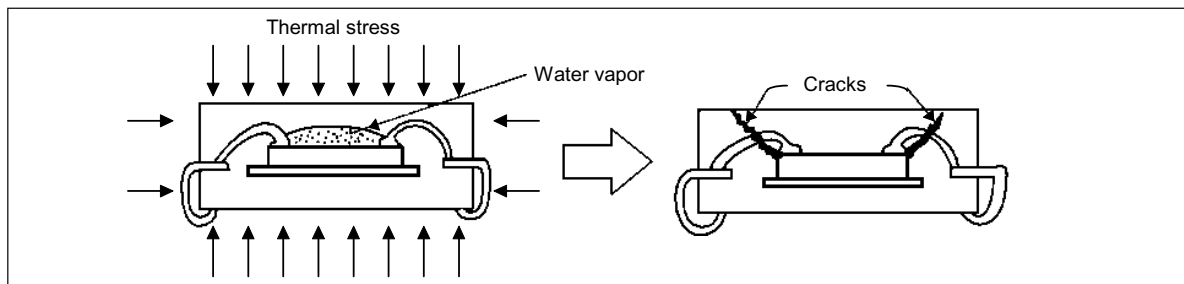


Figure 4.45 Package crack mechanism

5. Using Failure Analysis to Improve Reliability

As described in Section 4.1, the purpose of failure analysis is to achieve the high reliability required of a device. Therefore, failure analysis includes the following objectives:

- (1) Investigate failures that occur during evaluation of device prototypes and feed back the results to the design process so that reliability can be designed in at the development stage. In this way, improvements can be monitored to determine whether they are effective in the long term.
- (2) Investigate failures that occur during the manufacturing process and feed back the results to the manufacturing process so as to continuously maintain and improve quality and reliability during full production. In this way, improvements can be monitored to determine whether they are effective in the long term.
- (3) Investigate failures that occur in the field to determine whether they are true device failures or the result of some external factor brought about by inappropriate use, such as overvoltage, noise or thermal stress. If a true device failure has occurred, corrective action must be taken, tracing the product's history back to the manufacturing or design process. In this way, improvements can be monitored to determine whether they are effective in the long term.

Figure 5.1 illustrates the procedure for improving reliability using failure analysis.

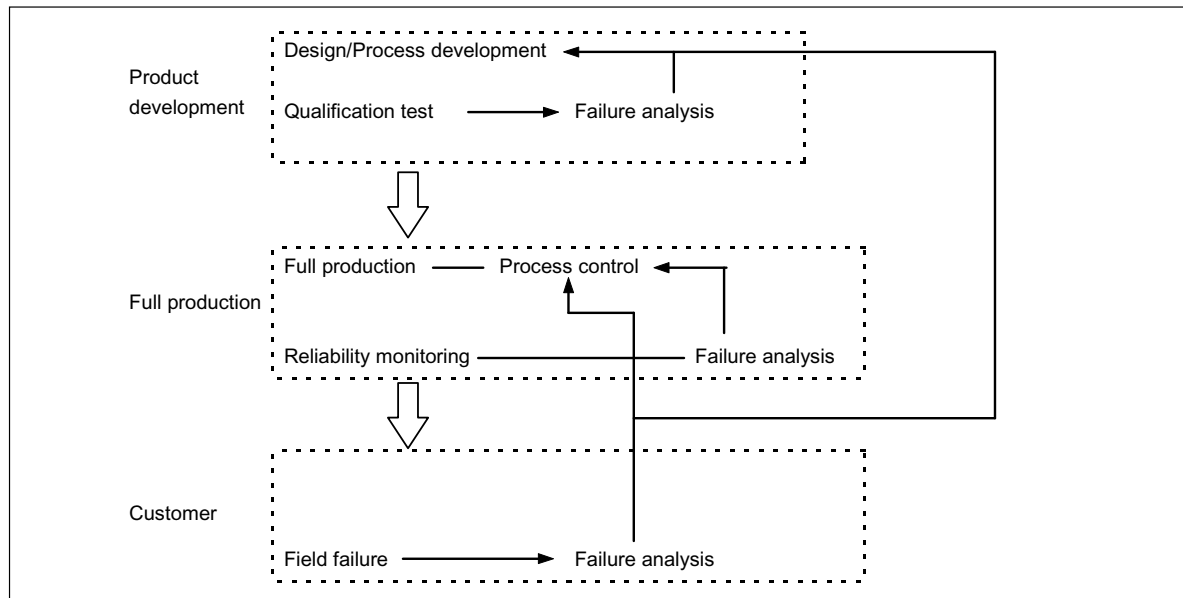


Figure 5.1 Procedure for improving reliability using failure analysis

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